



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/642,917	08/19/2000	Shiri Kadambi	108339-09055	8677
32294	7590	08/01/2005	EXAMINER	
SQUIRE, SANDERS & DEMPSEY L.L.P.			EMDADI, KAMRAN	
14TH FLOOR			ART UNIT	PAPER NUMBER
8000 TOWERS CRESCENT			2667	
TYSONS CORNER, VA 22182				

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/642,917

Applicant(s)

KADAMBI ET AL.

Examiner

Kamran Emdadi

Art Unit

2667

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Examiner submits that all previous grounds of rejection have been withdrawn and new grounds of rejection have been made as indicated below. Further, all indications made previously regarding allowable subject matter are hereby revoked in view of the new grounds of rejection. Claims 1-12, 14-23, 25-35, 37-38 and 40-42 are pending in the present application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 40-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrases "allocating memory locations between an internal memory and an external memory" and "from which the packet is to be transmitted" are indefinite.

The first phrase is indefinite because it is unclear to the Examiner how memory can be allocated between two separate memory locations when memory is normally allocated inside of a memory whether it is internal and external, more appropriate claim language may be "allocating [the same size or the same type of] memory locations in an external memory and in an internal memory"

The second phrase is indefinite because an egress port indicates an exit port and the term "from" indicates that the packet originated from the clustered network switch, however, the ending of the statement "which the packet is to be transmitted" implies the destination and not the original location of the packet before it is transmitted. More appropriate claim language may be "[to] which the packet is to be transmitted".

Claim 41 recites the limitation "a stack" on lines 13-15 and 18, however it is unclear (especially due to the phrase "the stack" on line 16) whether these references to "a stack" are separate stacks or are all the same stack in which case they terms on lines 14-15 and 18 should be changed to the stack. There is insufficient antecedent basis for this limitation in the claim. Claim 42 is also rejected by virtue of its dependency on claim 41.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6-10, 12, 14-22, 25-33, 35 and 37-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Muller et al. (U.S. Patent No. 6,246,680).

Regarding claims 1, 14-16, 20, 25-27, 31, 35 and 37-38 Muller teaches a data port interface supporting a plurality of nodes (see 205 of figure 2), a stack link interface 225 for communicating with other network switches (see figure 2) a CPU interface 215 communicating with a CPU 161 (see figure 2), a memory management unit 220 in communication with at least one data port interface and the stack link interface 225. Muller further teaches a memory interface between 220 and 230 that is in communication with a data port interface of 205 and a communication channel that communicates with 205, 225, 220 and 230, and where the memory manager 220 is configured to route data received to the memory interface of the memory 230 (see figure 3).

The configuration may also contain a mesh switch configuration for transmitting data between the switch fabric interfaces (e.g. 205 215 or 225) (see column 4, lines 10-15 and figure 2). Further, with regard to claim 15, it is inherent to have one less interface than the total number of building blocks so as to avoid any unnecessary interfaces not between building blocks. Furthermore, Muller teaches various data rate ports including Fast, Gigabit and regular Ethernet ports (see column 3, lines 50-55).

Regarding claims 2, 21-22 and 32-33, Muller teaches an internal memory interface for communicating with internal memory 320, 325 and 330 and communicating with a data port interface, and an external memory 230 interface with an external memory interface to the controller 330 (see figure 3 and column 8, lines 12-15 invoking additional support for a memory management system).

Regarding claim 3, Muller teaches a gigabit Ethernet interconnection to connect external switches having the same protocol (see column 3, lines 50-58).

Regarding claim 4, Muller teaches the same configuration noted above with regard to claim 3 with input and output data flow capability (see column 3, lines 50-55).

Regarding claim 6, Muller teaches a shared memory system that operates in accordance with a predetermined algorithm which is an inherent feature of a computer based system, in addition the memory configuration is a top down hierarchical memory system (see the memory blocks in figure 3).

Regarding claims 7-9, 17-18 and 28-29 Muller teaches various data rate ports including Fast, Gigabit and regular Ethernet ports (see column 3, lines 50-55).

Regarding claims 10 and 30, Muller teaches multi-layer switches (see column 4, lines 15-25).

Regarding claim 12, Muller teaches layer two switching (see column 3, lines 10-24 and column 5, lines 5-10).

Regarding claim 19, Muller teaches a mesh cluster of switch blocks (see column 4, lines 10-25).

Regarding claim 23, Muller teaches (see column 3, lines 50-55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2667

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 23 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Merchant et al. (U.S. Patent No. 6,775,290).

Muller teaches all of the above described features, however, is silent regarding a VLAN table coupled to a memory, as recited in claim 5, and using SRAM. Merchant teaches a switched communications network with a port of a network switch to connect multiple VLANs. The configuration of Merchant includes a VLAN table 118 and 120 in communication with a port 116 and a memory 114 (see figure 4). Further, SRAM is included in the network configuration (see figure 1).

Evidence to combine these references is evident from the background portion of their respective specifications. For instance, Muller discloses the need for a high performance network device building block for performing wire-speed multi-layer switching on N ports (see column 1, lines 35-39). Similarly, Merchant discloses the need to increase the flexibility of network switching. Both patents discuss gigabit Ethernet and multi-port handling of switched connections. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined these references and arrive at the features discussed in claims 5, 23 and 34.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Dobbins et al. (U.S. Patent No. 6,711,171).

Muller teaches all of the above described features, however, is silent regarding an ASIC chip solution to switching data over a network, as recited in claim 11. Dobbins

Art Unit: 2667

teaches a switched communications network with a configuration of VLAN switches that utilizes an ASIC chip.

Evidence to combine these references is evident from the background portion of their respective specifications. For instance, Muller discloses the need for a high performance network device building block for performing wire-speed multi-layer switching on N ports that linearly scales in performance with advances in silicon technology (see column 1, lines 35-39). Dobbins simply uses an ASIC chip as a means for accomplishing the network switched communications model disclosed therein. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined these references and arrive at the features discussed in claim 11.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kamran Emdadi whose telephone number is 571-272-6047. The examiner can normally be reached M-F between the hours of 8am-5pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2667

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kamran Emdadi

July 26, 2005


CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2667 7/27/05